

REMARKS

The Examiner objected to the drawings due to claims 11 and 12, which recited an in-circuit emulator. Accordingly, Applicants amended claims 11 and 12 to remove the “in-circuit emulator” term.

The Examiner rejected claims 1-3, 5-7, 9 and 10 under 35 U.S.C. §102(e) as being anticipated by United States Patent No. 6,403,448 of Reddy (“Reddy”); and rejected claims 4, 8 and 11-14 under 35 U.S.C. §103(a) as being unpatentable over Reddy. For the following reasons, Applicants assert that the all of claims 1-6 and 8-14 are allowable over Reddy.

Independent claim 1 has been amended to better clarify the novel and distinguishing features of the present invention. Both independent claims 1 and 11 now recite the unique feature of the present invention that the bond out chip include a pair of interconnected chips including a first chip that has an active core portion (e.g., the test portion of the bond out chip), and a second chip having a disabled core portion (e.g., the input/output portion of the bond out chip). Dependent claim 7 was canceled and dependent claim 8 was amended to depend from claim 1 rather than claim 7.

Independent claim 1 recites a bond out chip including a first chip with an active core portion, and a plurality of input/output pads that are located on at least one second chip and that are communicatively coupled to the first chip. The at least one second chip has a disabled core portion and is adjacent to the first chip. Claim 11 also recites a bond out chip that is formed by two adjacent chips, including one chip having an active core portion, and an adjacent chip that has a disabled core portion and input/output pads that are communicatively coupled to the first chip. Thus, the claimed inventions utilize a first active chip in combination with the input/output elements of a second disabled chip to form a bond out chip with accessible (e.g., spread out) input/output elements. These bond out

chips may be formed using “the same chips 10 that form standard production chips.” (Pending application at paragraph [030]). This allows the bond out chips to be formed in a cost-effective and efficient manner with a substantially identical set of masks as production chips and on the same wafer as production chips, thereby increasing production flexibility and reducing production costs. (Pending application at paragraph [030]).

Reddy does not teach forming a bond out chip (e.g., a test chip) using multiple chips including a first chip that is active and a second disabled chip that is connected to the active chip and used to provide I/O connectivity, as described in independent claims 1 and 11. Reddy teaches forming single mode chips that operates a single device mode, and multiple mode chips formed by multiple chips that are all active and operate together, as set forth below.

First, Reddy does not teach or disclose the production of bond out chips (i.e., test chips for use with in-circuit emulators). Reddy teaches forming chips including single device chips that operate in a single device mode, and multiple chips that operate together in a “multiple device” mode. In both cases, a standard production chip is formed, not a specialized test or bond out chip. In single device mode, the chips are cut into a section containing one chip, and in multiple device mode, the chips are cut into a section containing multiple devices. (Reddy, col. 4, lines 4-7). For example, in the single device mode, each chip may form a (x8) RAM device, and in double device mode the chips operate together to provide a (x16) RAM device. (Reddy, col. 4, lines 57-64). Thus, in both cases a standard operating chip is produced.

Importantly, Reddy teaches that when chips are grouped together in double device mode, the cores of both chips are active and operational. (Reddy, col. 4, lines 57-64, col. 5, lines 20-30). Reddy does **not** teach or suggest using a pair of chips together with one chip having an active core and the other chip having a disabled core and used only for its input/output elements, as recited in claims 1 and 11. In fact, Reddy specifically teaches away from using a disabled chip together with an active chip as recited in the claims. That is, Reddy teaches that in the event that a chip forming part of a multiple device is

determined to be defective, the data is used to saw the wafer apart to increase the single device yield, instead of forming a bond out chip using the active/disabled pair in the manner recited in the pending claims. (Reddy at col. 8, line 65 - col. 9, line 5).

Because Reddy does not disclose or suggest a bond out chip including the active core of a first chip and the input/output elements of a second disabled chip, Reddy cannot anticipate or render obvious claim 1 or 11. Furthermore, for at least these reasons, Reddy cannot anticipate nor render obvious any of claims 2-6, 8-10 or 12-14, which depend from claims 1 and 11.

CONCLUSIONS

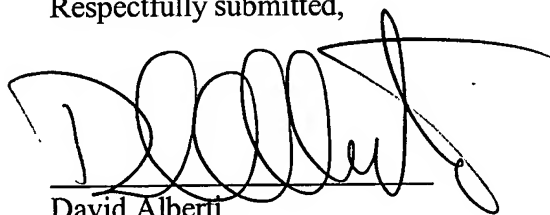
Applicants' claimed inventions are both novel and nonobvious over the prior art for the reasons set forth above. None of the prior art of record teaches each and every element of Applicants' claimed inventions.

For all of these reasons, Applicants respectfully assert that claims 1-6, and 8-14 are in condition for allowance. The Examiner's early reconsideration is respectfully requested.

If the Examiner has any questions, the Examiner is invited to contact Applicants' attorney at the following address or telephone number:

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Respectfully submitted,

A handwritten signature in black ink, appearing to read 'David Alberti', written over a horizontal line.

David Alberti
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